For horizontal scan frequencies of 80 kHz or above, only the first 32 of the 64 values stored for each row are accessed by the column address. In this mode, the signal HI-FREQ is low, and the clock signal WAVE-CLKB generates only 128 cycles in the active scan, instead of 256. This reduces the rate at which data is accessed from RAM, allowing operation at very high scan frequencies.

3.2.1.2 Alpha Circuit

The nine rows of values stored in RAM for each convergence waveform apply directly only to nine scan lines which lie on the boundaries of the eight vertical zones defined by U45. Convergence values for every scan line between these boundaries are synthesized on the fly by the output stage circuitry using linear interpolation. The signals required for this interpolation are provided by the alpha circuit.

Each vertical zone contains 1/8 of the total number of visible lines in the raster. This number (N) is written into an 8-bit "Zone" latch (U40) by the microprocessor and is updated whenever the number of lines in the raster changes, ie. for new horizontal and/or vertical scan frequencies. The outputs of the latch (N0-N7) are input to PLD U45 and EPROM U44. A vertical counter in U45 counts down from 'N' to 0, decrementing by one each scan line, then back up to 'N'. This is repeated until the V-DRIVE pulse resets the counter, completing four cycles in each video frame. The outputs of the counter (I0-I7) form a number 'I' which is input to U44.

EPROM U44 is a look-up table which inputs 'N' and 'I' as addresses and outputs 'I/N' (I divided by N) as 8-bit data. 'N' is the number of scan lines in a vertical zone. 'I' is the number of lines from the start of the current zone (or the end, depending on the direction of the vertical counter) at which the current scan line occurs. Therefore, 'I/N' represents the fractional position of the current scan line within the current zone.

The outputs of U44 (I/N0-I/N7) are fed to digital-to-analog converters U37 and U39. U37 produces two complementary current outputs which are converted to voltages by U300 to create H-ALPHA and H-ALPHA-I. H-ALPHA is a voltage representation of 'I/N'. H-ALPHA-I represents it's inverse, '1-I/N'. They are triangle waveforms of opposite phase with four complete cycles in each video frame. Both waveforms are summed together to create a DC offset voltage H-ALPHA-REF. The outputs of U39 are similarly processed to create V-ALPHA, V-ALPHA-I, and V-ALPHA-REF. The peak voltages from U37 and U39 are set by H-SIZE and V-SIZE, respectively, from I^2C octal DAC U79. These control voltages are made to track changes in horizontal and vertical raster size in order to reduce misconvergence effects.

A circuit consisting of flip-flop U43 and FETs Q1 and Q2 forces HSIZE and VSIZE to zero during power-up of the projector. When RESET* is driven low to reset the 68000 microprocessor, the flip-flop is cleared. This causes the FETs to conduct, forcing the outputs of the DACs to zero. This in turn forces the final convergence waveform outputs to zero volts. The software then initializes all convergence RAM values to 80H and writes to the "Zone" latch (U40). This strobes WR-NLATCH* low, which toggles the flip-flop and turns the FETs off, restoring the outputs of the DACs. This procedure prevents random waveforms from being output to the CVA before the RAMS can be initialized, which could cause excessive current draw from the amplifiers.

3.2.1.3 Output Stage

The output stage consists of six "waveform channels", two for each color. Each channel is composed of two latches, two 8-bit multiplying DACs and a quad op-amp IC. The circuits for the channels are nearly identical, therefore only the red horizontal channel will be described in detail.